AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application.

1. (currently amended) An integrated circuit comprising:

an interface including a first contact and a second contact;

a first transceiver coupled to the first contact;

a second transceiver coupled to the second contact;

wherein the integrated circuit is operable in a first mode and a second mode, wherein:

during the first mode of operation, the first transceiver ~~is capable of transmitting and receiving~~ transmits and receives signals and the second transceiver ~~is capable of transmitting and receiving~~ transmits and receives signals, wherein the integrated circuit operates in the first mode of operation in response to a control signal; and

during the second mode of operation, the first transceiver ~~is capable of only transmitting~~ transmits unidirectional signals and the second transceiver ~~is capable of only receiving~~ receives unidirectional signals, and

a control logic to output the control signal,

wherein the control signal is provided in response to a number of times the first transceiver transitions between transmitting signals and receiving signals during a period of time.

2. (cancelled)

3. (cancelled)

4. (currently amended) ~~The integrated circuit of claim 2~~ An integrated circuit comprising:

an interface including a first contact and a second contact;

a first transceiver coupled to the first contact;

a second transceiver coupled to the second contact;

wherein the integrated circuit is operable in a first mode and a second mode, wherein:

during the first mode of operation, the first transceiver transmits and receives signals and the second transceiver transmits and receives signals, wherein the integrated circuit operates in the first mode of operation in response to a control signal; and

during the second mode of operation, the first transceiver transmits unidirectional signals and the second transceiver receives unidirectional signals, and

a control logic to output the control signal,

wherein the control signal is provided ~~generated~~ in response to a number of transmit commands and a number of receive commands.

5. (currently amended) The integrated circuit of claim ~~42~~ 4 wherein the control signal is ~~generated~~ provided in response to a user selectable setting at initialization.

6. (currently amended) The integrated circuit of claim ~~42~~ 4 wherein the control signal is ~~generated~~ provided in response to a user selectable setting during normal operating mode.

7. (currently amended) The integrated circuit of claim 4 wherein the control signal is ~~generated~~ provided in response to a priority of the data.

8. (currently amended) The integrated circuit of claim ~~42~~ 4 wherein the control signal is ~~generated~~ provided in response to a number of transmit data packets and a number of receive data packets.

9. (currently amended) The integrated circuit of claim 8 wherein the control signal is ~~generated~~ provided in response to a priority of the data.

10. (currently amended) The integrated circuit of claim ~~42~~ 4 wherein the control logic is included in another integrated circuit and the control logic has information regarding bandwidth requirements.

11. (currently amended) The integrated circuit of claim ~~42~~ 4 wherein the control logic includes executable instructions.

12. (original) The integrated circuit of claim 11 wherein the executable instructions are included in an application software program.

13. (original) The integrated circuit of claim 11 wherein the executable instructions are included in an operating software program.

14. (original) The integrated circuit of claim 11 wherein the executable instructions are included in firmware.

15. (currently amended) The integrated circuit of claim ~~42~~ 42 wherein the control signal is ~~generated~~ provided in response to a number of data packets waiting to be transmitted.

16. (currently amended) The integrated circuit of claim ~~42~~ 42 wherein the control signal is ~~generated~~ provided in response to a number of data packets waiting to be received.

17. (currently amended) ~~The integrated circuit of claim 2~~ An integrated circuit comprising:

an interface including a first contact and a second contact;

a first transceiver coupled to the first contact;

a second transceiver coupled to the second contact;

wherein the integrated circuit is operable in a first mode and a second mode, wherein:

during the first mode of operation, the first transceiver transmits and receives signals and the second transceiver transmits and receives signals, wherein the integrated circuit operates in the first mode of operation in response to a control signal; and

during the second mode of operation, the first transceiver transmits unidirectional signals and the second transceiver receives unidirectional signals, and

a control logic to output the control signal,

wherein the control signal is ~~generated~~ provided in response to an average time a data packet waits to be transmitted.

18. (currently amended) ~~The integrated circuit of claim 2~~ An integrated circuit comprising:

an interface including a first contact and a second contact;

a first transceiver coupled to the first contact;

a second transceiver coupled to the second contact;

wherein the integrated circuit is operable in a first mode and a second mode, wherein:

during the first mode of operation, the first transceiver transmits and receives signals and the second transceiver transmits and receives signals, wherein the integrated circuit operates in the first mode of operation in response to a control signal; and

during the second mode of operation, the first transceiver transmits unidirectional signals and the second transceiver receives unidirectional signals, and

a control logic to output the control signal,

wherein the control signal is ~~generated~~ provided in response to a power consumption of the integrated circuit.

19. (currently amended) ~~The integrated circuit of claim 2~~ An integrated circuit comprising:

an interface including a first contact and a second contact;

a first transceiver coupled to the first contact;

a second transceiver coupled to the second contact;

wherein the integrated circuit is operable in a first mode and a second mode, wherein:

during the first mode of operation, the first transceiver transmits and receives signals and the second transceiver transmits and receives signals, wherein the integrated circuit operates in the first mode of operation in response to a control signal; and

during the second mode of operation, the first transceiver transmits unidirectional signals and the second transceiver receives unidirectional signals, and

a control logic to output the control signal,

wherein the control signal is ~~generated~~ provided in response to a temperature of the integrated circuit.

20. (currently amended) ~~The integrated circuit of claim 2~~ An integrated circuit comprising:

an interface including a first contact and a second contact;

a first transceiver coupled to the first contact;

a second transceiver coupled to the second contact;

wherein the integrated circuit is operable in a first mode and a second mode, wherein:

during the first mode of operation, the first transceiver transmits and receives signals and the second transceiver transmits and receives signals, wherein the integrated circuit operates in the first mode of operation in response to a control signal; and

during the second mode of operation, the first transceiver transmits unidirectional signals and the second transceiver receives unidirectional signals, and

a control logic to output the control signal,

wherein the control signal is ~~generated~~ provided in response to a first statistic obtained during a first period of time and a second statistic obtained during a second period of time.

21. (currently amended) ~~The integrated circuit of claim 2~~ An integrated circuit comprising:

an interface including a first contact and a second contact;

a first transceiver coupled to the first contact;

a second transceiver coupled to the second contact;

wherein the integrated circuit is operable in a first mode and a second mode, wherein:

during the first mode of operation, the first transceiver transmits and receives signals and the second transceiver transmits and receives signals, wherein the integrated circuit operates in the first mode of operation in response to a control signal; and

during the second mode of operation, the first transceiver transmits unidirectional signals and the second transceiver receives unidirectional signals, and

a control logic to output the control signal,

wherein the integrated circuit ~~is capable of generating~~ provides a first bandwidth request and another integrated circuit ~~is capable of generating~~ provides a second bandwidth request, and wherein the control signal is ~~generated~~ provided in response to the first bandwidth request and the second bandwidth request.

22. (currently amended) ~~The integrated circuit of claim 2~~ An integrated circuit comprising:

an interface including a first contact and a second contact;

a first transceiver coupled to the first contact;

a second transceiver coupled to the second contact;

wherein the integrated circuit is operable in a first mode and a second mode, wherein:

during the first mode of operation, the first transceiver transmits and receives signals and the second transceiver transmits and receives signals, wherein the integrated circuit operates in the first mode of operation in response to a control signal; and

during the second mode of operation, the first transceiver transmits unidirectional signals and the second transceiver receives unidirectional signals, and

a control logic to output the control signal,

wherein the integrated circuit ~~is capable of generating~~ provides a first temperature signal representing the temperature of the integrated circuit and another integrated circuit ~~is capable of generating~~ provides a second temperature signal representing the temperature of another integrated circuit, and wherein the control signal is ~~generated~~ provided in response to the first temperature signal and the second temperature signal.

23. (currently amended) The integrated circuit of claim ~~42~~ 42 wherein the control signal is ~~generated~~ provided periodically.

24. (currently amended) The integrated circuit of claim ~~42~~ 42 wherein the control logic ~~generates~~ provides ~~a~~ the control signal in response to an override signal.

25. (currently amended) ~~The integrated circuit of claim 2~~ An integrated circuit comprising:

an interface including a first contact and a second contact;

a first transceiver coupled to the first contact;

a second transceiver coupled to the second contact;

wherein the integrated circuit is operable in a first mode and a second mode, wherein:

during the first mode of operation, the first transceiver transmits and receives signals and the second transceiver transmits and receives signals, wherein the integrated circuit operates in the first mode of operation in response to a control signal; and

during the second mode of operation, the first transceiver transmits unidirectional signals and the second transceiver receives unidirectional signals, and

a control logic to output the control signal,

wherein the control logic ~~generates~~ outputs ~~a~~ the control signal in response to a threshold value that represents a minimum bandwidth.

26. (cancelled)

27. (currently amended) ~~The integrated circuit of claim 25 wherein~~ An integrated circuit comprising:

an interface including a first contact and a second contact;

a first transceiver coupled to the first contact;

a second transceiver coupled to the second contact;

wherein the integrated circuit is operable in a first mode and a second mode, wherein:

during the first mode of operation, the first transceiver transmits and receives signals and the second transceiver transmits and receives signals, wherein the integrated circuit operates in the first mode of operation in response to a control signal; and

during the second mode of operation, the first transceiver transmits unidirectional signals and the second transceiver receives unidirectional signals, and

a control logic to output the control signal,

wherein the control logic outputs the control signal in response to ~~the~~ a threshold value ~~is~~ that represents a maximum temperature value.

28. (currently amended) ~~The integrated circuit of claim 25 wherein~~ An integrated circuit comprising:

an interface including a first contact and a second contact;

a first transceiver coupled to the first contact;

a second transceiver coupled to the second contact;

wherein the integrated circuit is operable in a first mode and a second mode, wherein:

during the first mode of operation, the first transceiver transmits and receives signals and the second transceiver transmits and receives signals, wherein the integrated circuit operates in the first mode of operation in response to a control signal; and

during the second mode of operation, the first transceiver transmits unidirectional signals and the second transceiver receives unidirectional signals, and

a control logic to output the control signal,

wherein the control logic outputs the control signal in response to ~~the~~ a threshold value ~~is~~ that represents a maximum power consumption value.

29. (cancelled)

30. (currently amended) ~~The integrated circuit of claim 25 wherein~~ An integrated circuit comprising:

an interface including a first contact and a second contact;

a first transceiver coupled to the first contact;

a second transceiver coupled to the second contact;

wherein the integrated circuit is operable in a first mode and a second mode, wherein:

during the first mode of operation, the first transceiver transmits and receives signals and the second transceiver transmits and receives signals, wherein the integrated circuit operates in the first mode of operation in response to a control signal; and

during the second mode of operation, the first transceiver transmits unidirectional signals and the second transceiver receives unidirectional signals, and

a control logic to output the control signal,

wherein the control logic outputs a control signal in response to ~~the~~ a threshold value ~~is~~ that represents a minimum latency value.

31. (currently amended) The integrated circuit of claim ~~42~~ 4 wherein the integrated circuit is operable in a third mode,

wherein:

during the third mode of operation, the first transceiver ~~is capable of transmitting and receiving~~ transmits and receives signals and the second transceiver is disabled ~~for transmitting or receiving~~ to transmit and receive signals.

32. (original) The integrated circuit of claim 31 wherein the third mode of operation is a phase calibration mode.

33. (original) The integrated circuit of claim 31 wherein the third mode of operation is an impedance calibration mode.

34. (original) The integrated circuit of claim 31 wherein the second transceiver is disabled responsive to power constraint.

35. (original) The integrated circuit of claim 31 wherein the second transceiver is disabled in response to a hardware device failure.

36. (original) The integrated circuit of claim 31 wherein the second transceiver is disabled in response to a signal failure.

37. (currently amended) The integrated circuit of claim 42 wherein the integrated circuit is operable in a third mode,

wherein:

during the third mode of operation, the first transceiver ~~is capable of only transmitting~~ transmits unidirectional signals and the second transceiver is disabled.

38. (currently amended) The integrated circuit of claim 42 wherein the integrated circuit is operable in a third mode,

wherein:

during the third mode of operation, the first transceiver ~~is capable of only receiving~~ receives unidirectional signals and the second transceiver is disabled.

39. (original) The integrated circuit of claim 38 wherein the third mode of operation is a phase calibration mode.

40. (original) The integrated circuit of claim 38 wherein the third mode of operation is an impedance calibration mode.

41. (cancelled)

42. (currently amended) The integrated circuit of claim 42 wherein the first transceiver and second transceiver are coupled to an input multiplex deserializer circuit and an output multiplex serializer circuit.

43.-62. (cancelled)